have been made to the previous version of the claims by the current response, the clean set is followed by a marked-up version indicating the changes made (see 37 CFR 1.121(c)(3)).

Sub E7

C1

1. (TWICE AMENDED) An apparatus comprising:

one or more logic circuits configured to provide logical operation, wherein said one or more logic circuits comprise (i) programmable logic elements and (ii) non-programmable logic elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

2. The apparatus according to claim 1, wherein said one or more logic circuits comprise variable width logic circuits.

3. The apparatus according to claim 2, wherein a width of each of said one or more logic circuits is determined in response to one or more input signals.

4. The apparatus according to claim 1, wherein each of said one or more logic circuits is configured to receive a first one or more inputs, wherein said first one or more inputs comprise

multi-bit or single-bit signals in a serial or a parallel configuration.

5. (AMENDED) The apparatus according to claim 1, wherein one or more of said logic circuits comprises a hard wired multiplier.

6. (AMENDED) The apparatus according to claim 1, wherein one or more of said logic circuits are configured to perform a cyclic redundancy check (CRC) functions.

7. (AMENDED) The apparatus according to claim 1, wherein one or more of said logic circuits is configured to present an output.

8. (AMENDED) The apparatus according to claim 7, wherein each of said one or more outputs comprise intermediate signals.

9. The apparatus according to claim 7, further comprising:

an adder circuit configured to receive said one or more outputs.

10. (THREE TIMES AMENDED) The apparatus according to claim 1, wherein said routable interconnect circuit is configured to route signals to/from one or more of said non-programmable elements.

11. (AMENDED) The apparatus according to claim 10, further comprising a number of registers configured to increase a throughput of said one or more logic circuits.

12. The apparatus according to claim 1, wherein each of said one or more logic circuits comprise an input portion configured to store one or more input signals.

13. The apparatus according to claim 12, wherein each of said one or more logic circuits comprises an output portion configured to store an output.

15. (TWICE AMENDED) An apparatus comprising:

means for receiving one or more input signals; and

means for performing logical operation on said input signals using (i) programmable logic elements and (ii) non-programmable logic elements within a programmable logic device (PLD), wherein said programmable logic elements are (i)

configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

16. (TWICE AMENDED) A method for computing in a programmable logic device (PLD) comprising the steps of:

(A) receiving one or more input signals;

(B) performing logical operation on said one or more input signals with (i) programmable logic elements and (ii) non-programmable logic elements within said programmable logic device, wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

17. (TWICE AMENDED) The method according to claim 16, further comprising the step of:

(C) generating one or more output signals.

18. (AMENDED) The method according to claim 16, wherein step (B) further comprises:

multiplying said one or more input signals.

19. (AMENDED) The method according to claim 17, wherein step (B) further comprises:

receiving said one or more outputs and adding said one or more outputs.

20. (TWICE AMENDED) The method according to claim 17, wherein step (C) further comprises:

routing said one or more outputs with said routable interconnect circuit.

C1 cont'd

21. The apparatus according to claim 1, wherein said non-programmable elements comprise dedicated logic having a specific functionality.

22. The apparatus according to claim 1, wherein said programmable elements comprise configurable macrocells.

Please add the following new claims:

23. (NEW) The apparatus according to claim 1, further comprising:

one or more first registers configured to couple one or more input signals to said non-programmable logic elements; and

C2 5

one or more second registers configured to receive one or more output signals from said non-programmable logic elements.

C2 cont

24. (NEW) The apparatus according to claim 1, wherein said non-programmable logic elements (i) comprise hard wired multipliers having a first width and (ii) are couplable to form one or more multipliers having a second width.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

10. (THREE TIMES AMENDED) The apparatus according to claim [9] 1, wherein said routable interconnect circuit is configured to route signals to/from one or more of said non-programmable elements.

17. (TWICE AMENDED) The method according to claim 16, further comprising the step of:

(C) generating one or more [intermediate] output signals.

18. (AMENDED) The method according to claim [17] 16, wherein step [(C)] (B) further comprises:

multiplying said one or more input signals.

19. (AMENDED) The method according to claim [16] 17, wherein step (B) further comprises:

receiving said one or more outputs and adding said one or more outputs.

20. (TWICE AMENDED) The method according to claim [16] 17, wherein step [(B)] (C) further comprises:

routing said one or more outputs with said routable interconnect circuit.

23. (NEW) The apparatus according to claim 1, further comprising:

one or more first registers configured to couple one or more input signals to said non-programmable logic elements; and

one or more second registers configured to receive one or more output signals from said non-programmable logic elements.

24. (NEW) The apparatus according to claim 1, wherein said non-programmable logic elements (i) comprise hard wired multipliers having a first width and (ii) are couplable to form one or more multipliers having a second width.